DUAL DIGITAL ISOLATORS

FEATURES

- 1, 5, 25, and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1 ns max
  - Low Pulse-Width Distortion (PWD); 1 ns max
  - Low Jitter Content; 1 ns Typ at 150 Mbps
- Typical 25-Year Life at Rated Voltage (see app. note SLLA197 and Figure 20)
- 4000-V_{peak} Isolation, 560 V peak V_{IORM}
  - UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1
  - 50 kV/µs Typical Transient Immunity
- Operates with 3.3-V or 5-V Supplies
- 4 kV ESD Protection
- High Electromagnetic Immunity
- –40°C to 125°C Operating Range

APPLICATIONS

- Industrial Fieldbus
  - Modbus
  - Profibus™
  - DeviceNet™ Data Buses
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION

The ISO7220 and ISO7221 are dual-channel digital isolators. To facilitate PCB layout, the channels are oriented in the same direction in the ISO7220 and in opposite directions in the ISO7221. These devices have a logic input and output buffer separated by TI's silicon-dioxide (SiO_2) isolation barrier, providing galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

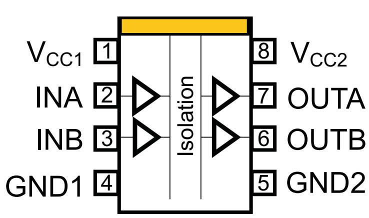
A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received every 4 µs, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state.

The small capacitance and resulting time constant provide fast operation with signaling rates available from 0 Mbps (dc) to 150 Mbps.(1) The A-, B- and C-option devices have TTL input thresholds and a noise filter at the input that prevents transient pulses from being passed to the output of the device. The M-option devices have CMOS $V_{CC}/2$ input thresholds and do not have the input noise-filter and the additional propagation delay.

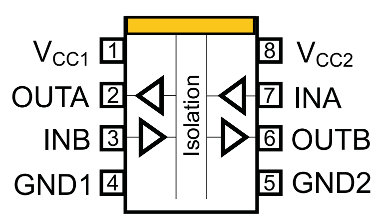
These devices require two supply voltages of 3.3 V, 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

ISO7220xD



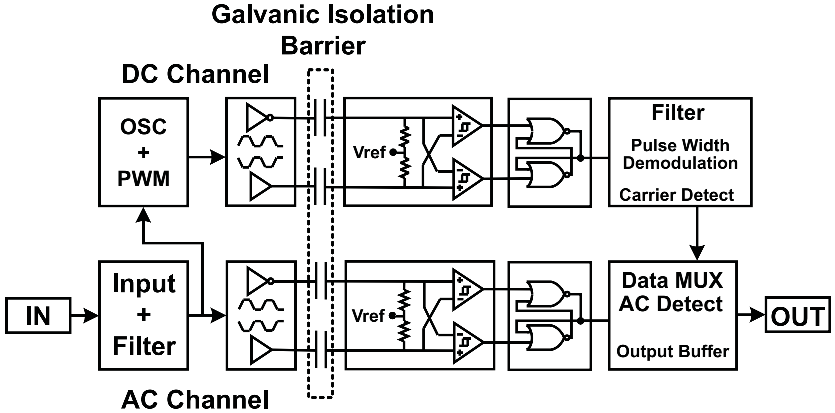
ISO7221xD



(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SINGLE-CHANNEL FUNCTION DIAGRAM



AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	PACKAGE	INPUT THRESHOLD	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7220A	1 Mbps	SOIC-8	≈ 1.5 V (TTL) (CMOS compatible)	Same direction	I7220A	ISO7220AD (rail)
						ISO7220ADR (reel)
ISO7220B	5 Mbps	SOIC-8	≈ 1.5 V (TTL) (CMOS compatible		I7220B	ISO7220BD (rail)
						ISO7220BDR (reel)
ISO7220C	25 Mbps	SOIC-8	≈ 1.5 V (TTL) (CMOS compatible)		I7220C	ISO7220CD (rail)
						ISO7220CDR (reel)
ISO7220M	150 Mbps	SOIC-8	$V_{CC}/2$ (CMOS)		I7220M	ISO7220MD (rail)
						ISO7220MDR (reel)
ISO7221A	1 Mbps	SOIC-8	≈ 1.5 V (TTL) (CMOS compatible)	Opposite directions	I7221A	ISO7221AD (rail)
						ISO7221ADR (reel)
ISO7221B	5 Mbps	SOIC-8	≈ 1.5 V (TTL) (CMOS compatible)		I7221B	ISO7221BD (rail)
						ISO7221ABR (reel)
ISO7221C	25 Mbps	SOIC-8	≈ 1.5 V (TTL) (CMOS compatible)		TI7221C	ISO7221CD (rail)
						ISO7221CDR (reel)
ISO7221M	150 Mbps	SOIC-8	$V_{CC}/2$ (CMOS)		I7221M	ISO7221MD (rail)
						ISO7221MDR (reel)

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program (1)
File Number: 40016131	File Number: 1698195	File Number: E181974

(1) Production tested ≥3000 VRMS for 1 second in accordance with UL 1577.

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 to 6	V
V_I	Voltage at IN, OUT				–0.5 to 6	V
I_O	Output current				±15	mA
ESD	Electrostatic discharge	Human Body Model	Electrostatic discharge JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				170	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(1), V_{CC1}, V_{CC2}		3		5.5	V
I_{OH}	High-level output current				4	mA
I_{OL}	Low-level output current		–4			mA
t_{ui}	Input pulse width	ISO722xA	1	0.67		µs
		ISO722xB	200	100		
		ISO722xC	40	33		ns
		ISO722xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO722xA	0	1500	1000	kbps
		ISO722xB	0	10	5	Mbps
		ISO722xC	0	30	25	Mbps
		ISO722xM	0	200(2)	150	
V_{IH}	High-level input voltage	ISO722xA, ISO722xC	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IH}	High-level input voltage	ISO722xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.3 V_{CC}	V
T_J	Junction temperature		–40		150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 & IEC 61000-4-9 certification				1000	A/m

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.
(2) Typical sigalling rate under ideal conditions at 25°C.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		1	2	mA
	ISO7221				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		2	3	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		4	9	
	ISO7221C, ISO7221M				12	22	
I_{CC2}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		16	31	
	ISO7221x				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		17	32	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		20	34	
	ISO7221C, ISO7221M				12	22	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8	4.6		V
			I_{OH} = –20 μA, See Figure 1	V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1		0.2	0.4	V
			I_{OL} = 20 μA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	μA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 3	25	50		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO722xA	See Figure 1	280	405	475	ns
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				1	14	
t_{PLH}, t_{PHL}	Propagation delay	ISO722xB		42	55	70	
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				1	3	
t_{PLH}, t_{PHL}	Propagation delay	ISO722xC		22	32	42	
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				1	2	
t_{PLH}, t_{PHL}	Propagation delay	ISO722xM		6	10	16	
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				0.5	1	
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				180	ns
		ISO722xB				17	
		ISO722xC				10	
		ISO722xM				3	

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	ns
		ISO722xB			0.6	3	
		ISO722xC/M			0.2	1	
t_r	Output signal rise time		See Figure 1		1		ns
t_f	Output signal fall time				1		
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 4, Figure 17		1		ns
			150 Mbps unrestricted bit run length data input, both channels, See Figure 4		2		

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		1	2	mA
	ISO7221x				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		2	3	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		4	9	
	ISO7221C, ISO7221M				12	22	
I_{CC2}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		8	18	
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		9	19	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		10	20	
	ISO7221C, ISO7221M				6	12	
V_{OH}	High-level output voltage	ISO7220x	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4			V
		ISO7221x (5-V side)		V_{CC} – 0.8			
			I_{OH} = –20 µA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1			0.4	V
			I_{OL} = 20 µA, See Figure 1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 3	15	40		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5 V, V_{CC2} at 3.3 V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA	See Figure 1	285	410	480	ns
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				1	14	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xB		45	58	75	
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				1	3	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC		25	36	48	
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				1	2	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xM		7	12	20	
PWD	Pulse-width distortion $\|t_{pHL} - t_{pLH}\|$ (1)				0.5	1	
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				180	ns
		ISO722xB				17	
		ISO722xC				10	
		ISO722xM				5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	
		ISO722xB			0.6	3	
		ISO722xC/M			0.2	1	
t_r	Output signal rise time		See Figure 1		2		ns
t_f	Output signal fall time				2		
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 4, Figure 17		1		ns
			150 Mbps unrestricted bit run length data input, both channels, See Figure 4		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		0.6	1	mA
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		1	2	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		2	4	
	ISO7221C, ISO7221M				6	12	
I_{CC2}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		16	31	
	ISO7221x				8.5	17	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		18	32	
	ISO7221A, ISO7221B				10	18	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		20	34	
	ISO7221C, ISO7221M				12	22	
V_{OH}	High-level output voltage	ISO7220x	I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.8			V
		ISO7221x (3.3-V side)		V_{CC} – 0.4			
			I_{OH} = –20 μA, See Figure 1	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		IOL = 4 mA, See Figure 1			0.4	
			IOL = 20 μA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 3	15	40		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3 V, V_{CC2} at 5 V OPERTAION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA	See Figure 1	285	395	480	ns
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				1	18	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xB		45	58	75	
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				1	4	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC		25	36	48	
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				1	3	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xM		7	12	21	
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				0.5	1	
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				190	
		ISO722xB				17	
		ISO722xC				10	
		ISO722xM				5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	
		ISO722xB			0.6	3	
		ISO7220C/M			0.2	1	
t_r	Output signal rise time		See Figure 1		1		
t_f	Output signal fall time				1		
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 4, Figure 17		1		ns
			150 Mbps unrestricted bit run length data input, both channels, See Figure 4		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		0.6	1	mA
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		1	2	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		2	4	
	ISO7221C, ISO7221M				6	12	
I_{CC2}	ISO7220x	Quiescent	$V_I = V_{CC}$ or 0 V, no load		8	18	
	ISO7221x				4.3	9.5	
	ISO7220A, ISO7220B	1 Mbps	$V_I = V_{CC}$ or 0 V, no load		9	19	
	ISO7221A, ISO7221B				5	11	
	ISO7220C, ISO7220M	25 Mbps	$V_I = V_{CC}$ or 0 V, no load		10	20	
	ISO7221C, ISO7221M				6	12	
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 1	V_{CC} – 0.4	3		V
			I_{OH} = –20 μA, See Figure 1	V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 1		0.2	0.4	
			I_{OL} = 20 μA, See Figure 1		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	μA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at V_{CC}, V_I = 0.4 sin (4E6πt)		1		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V, See Figure 3	15	40		kV/μs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3 V to 3.6 V.

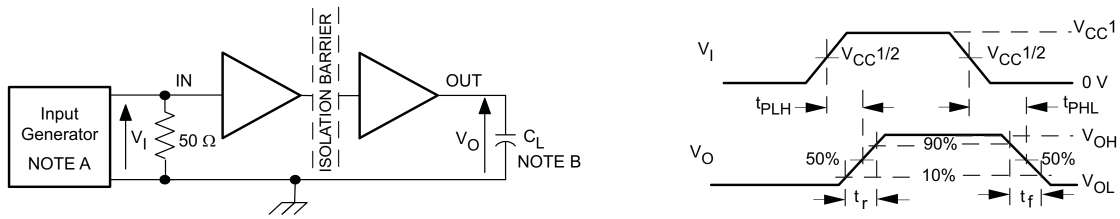
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V operation, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay	ISO722xA	See Figure 1	290	400	485	ns
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				1	18	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xB		46	62	78	
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				1	4	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xC		26	40	52	
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				1	3	
t_{pLH}, t_{pHL}	Propagation delay	ISO722xM		8	16	25	
PWD	Pulse-width distortion $\|t_{pHL} – t_{pLH}\|$ (1)				0.5	1	
$t_{sk(pp)}$	Part-to-part skew (2)	ISO722xA				190	
		ISO722xB				17	
		ISO722xC				10	
		ISO722xM				5	
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO722xA			3	15	
		ISO722xB			0.6	3	
		ISO722xC/M			0.2	1	
t_r	Output signal rise time		See Figure 1		2		
t_f	Output signal fall time				2		
t_{fs}	Failsafe output delay time from input power loss		See Figure 2		3		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO722xM	150 Mbps PRBS NRZ data, 5-bit max same polarity input, both channels, See Figure 4, Figure 17		1		ns
			150 Mbps unrestricted bit run length data input, both channels, See Figure 4		2		

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

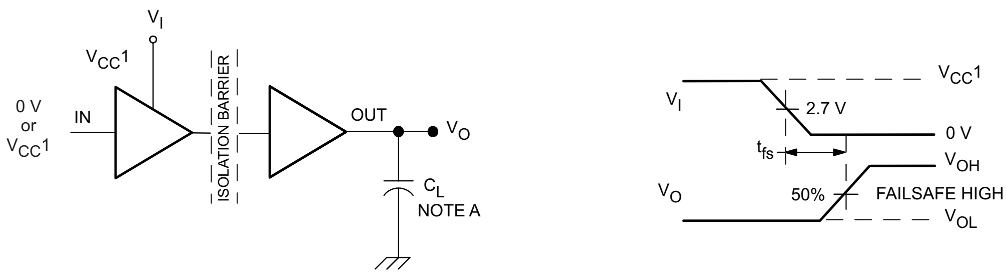
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

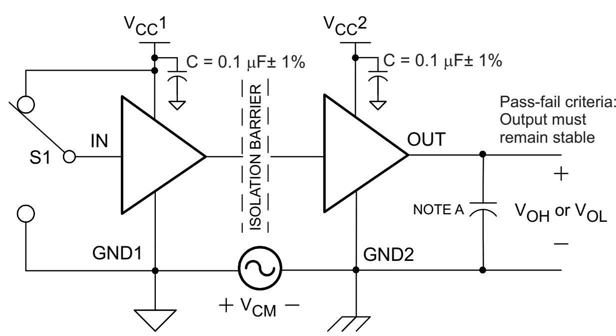
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



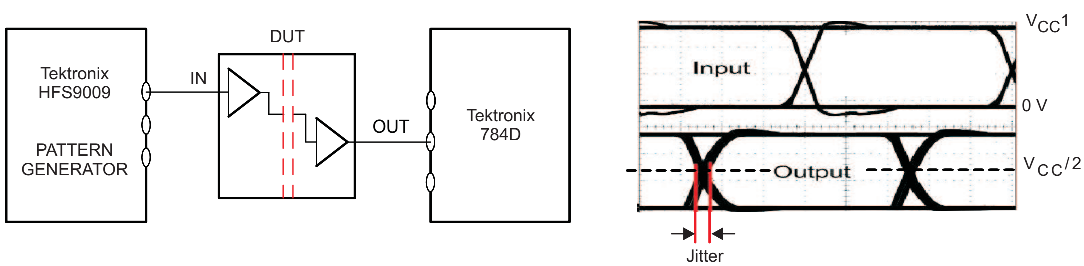
A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit



NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps.

Figure 4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

DEVICE INFORMATION

IEC PACKAGE CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	SOIC-8	4.8			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	SOIC-8	4.3			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1		≥175			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation		0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C			$>10^{12}$		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ max			$>10^{11}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)			1		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)			1		pF

NOTE: Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the *Isolation Glossary*. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC 60664-1 RATINGS TABLE

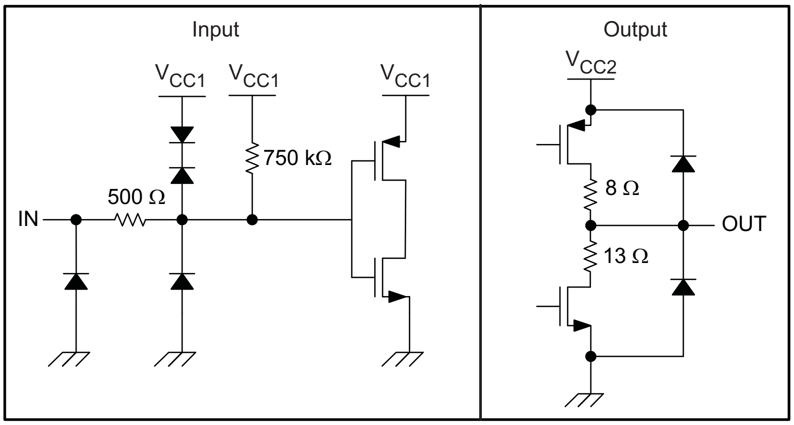
PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III
	Rated mains voltage ≤400 VRMS	I-II

IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input to output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1 s, Partial discharge <5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

DEVICE I/O SCHEMATICS



IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	SOIC-8	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			124	mA
			θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			190	
T_S	Maximum case temperature	SOIC-8				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

SOIC-8 PACKAGE THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air		Low-K Thermal Resistance(1)		212		°C/W
			High-K Thermal Resistance		122		
θ_{JB}	Junction-to-Board Thermal Resistance				37		
θ_{JC}	Junction-to-Case Thermal Resistance				69.1		
P_D	Device Power Dissipation	ISO722xM	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, Input a 150 Mbps 50% duty cycle square wave			390	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

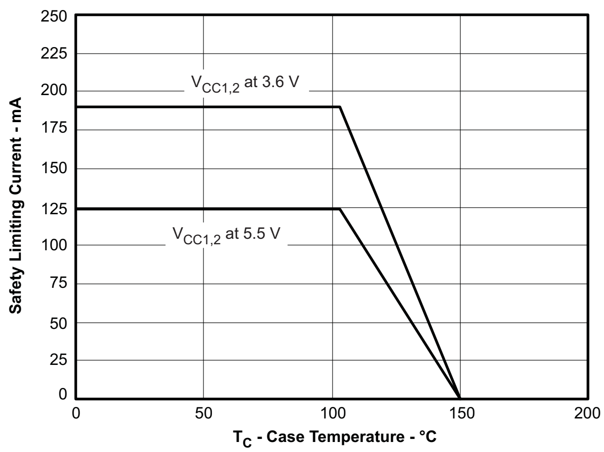


Figure 5. SOIC-8 θ_{JC} THERMAL DERATING CURVE per IEC 60747-5-2

DEVICE FUNCTION TABLE

Table 1. ISO7220x or ISO7221x(1)

INPUT SIDE V_{CC}	OUTPUT SIDE V_{CC}	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up(Vcc ≥ 3.0V); PD = Powered Down (Vcc ≤ 2.5V); X = Irrelevant; H = High Level; L = Low Level

TYPICAL CHARACTERISTIC CURVES

3.3-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

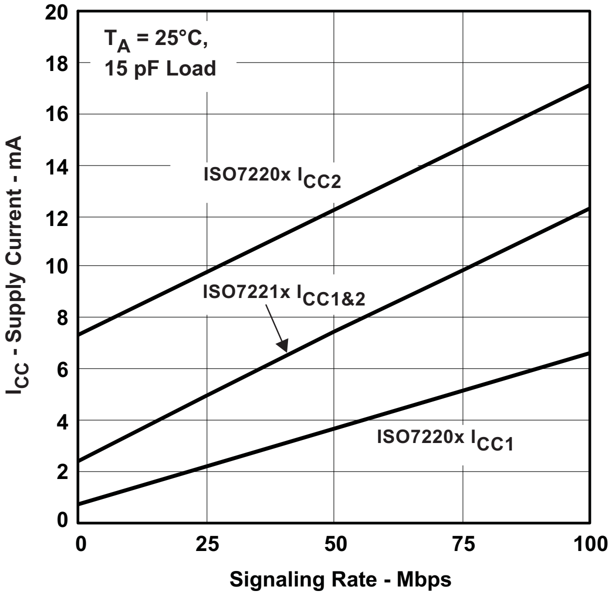


Figure 6.

5-V RMS SUPPLY CURRENT vs SIGNALING RATE (Mbps)

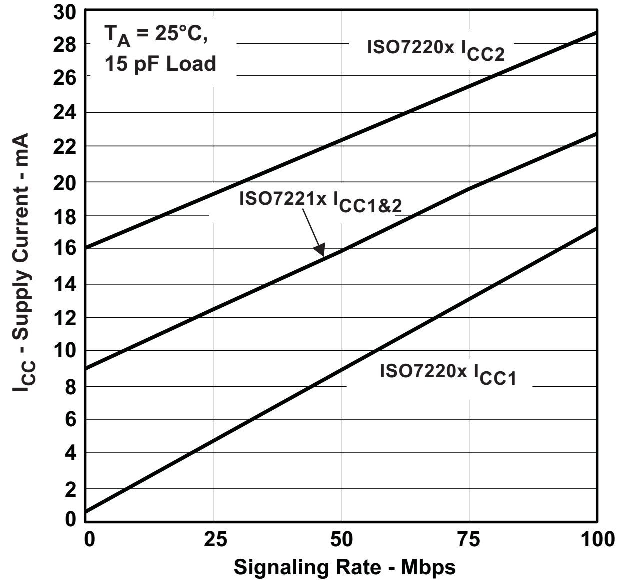


Figure 7.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE, ISO722xA

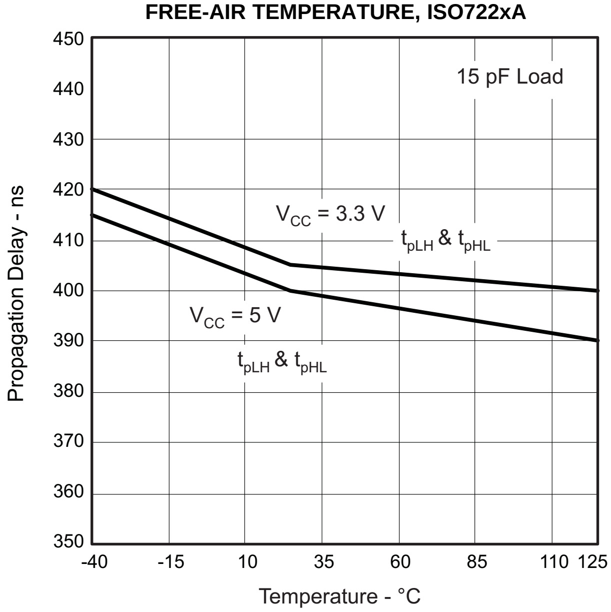


Figure 8.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE, ISO722xB

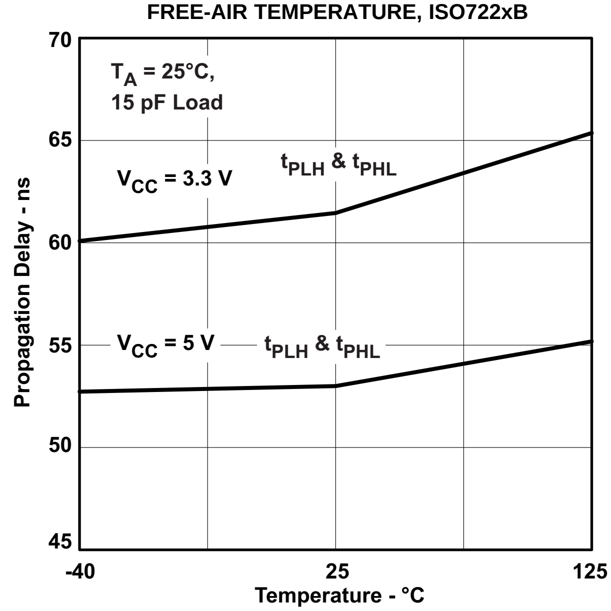


Figure 9.

TYPICAL CHARACTERISTIC CURVES (continued)

PROPAGATION DELAY vs FREE-AIR TEMPERATURE, ISO722xC

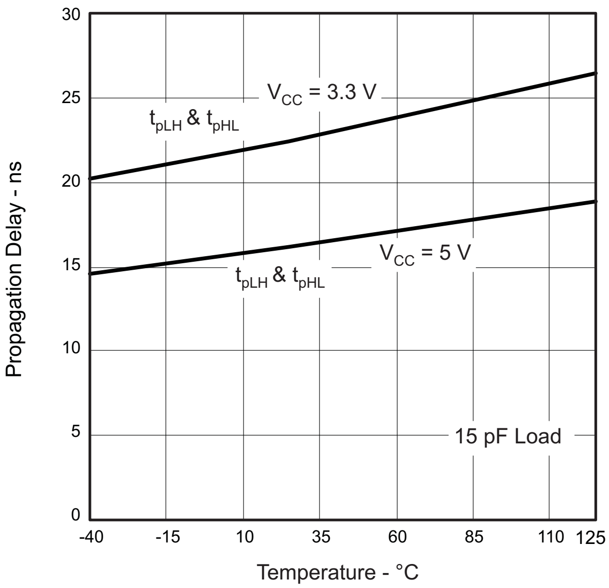


Figure 10.

PROPAGATION DELAY vs FREE-AIR TEMPERATURE, ISO722xM

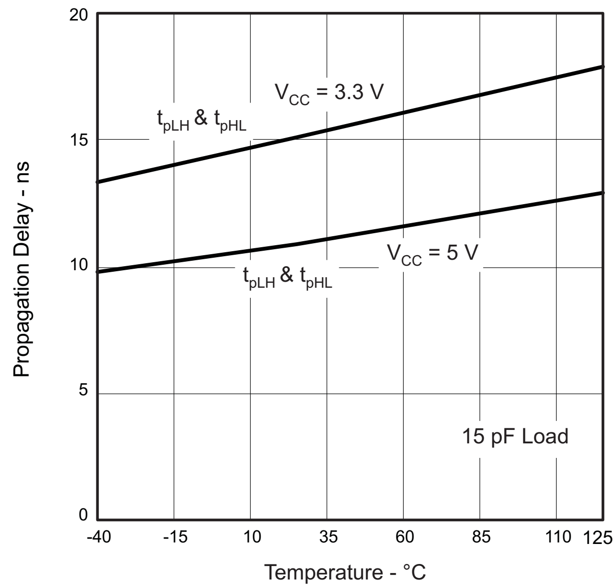


Figure 11.

ISO722xA, ISO722xB AND ISO722xC INPUT VOLTAGE LOW-TO-HIGH SWITCHING THRESHOLD vs FREE-AIR TEMPERATURE

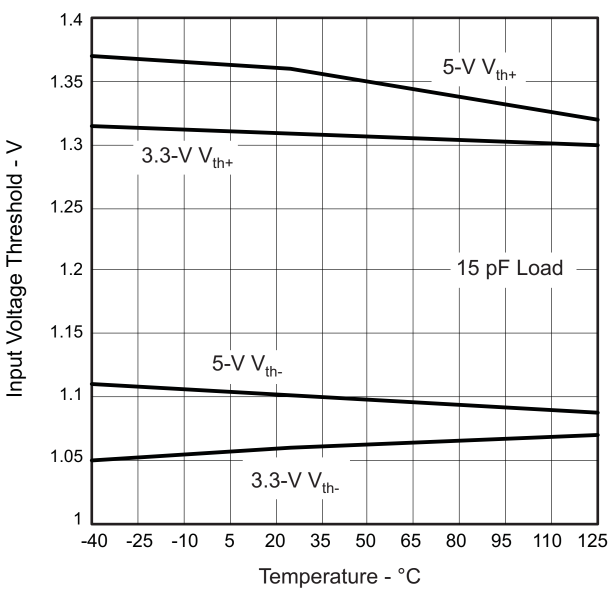


Figure 12.

ISO722xM INPUT VOLTAGE HIGH-TO-LOW vs FREE-AIR TEMPERATURE

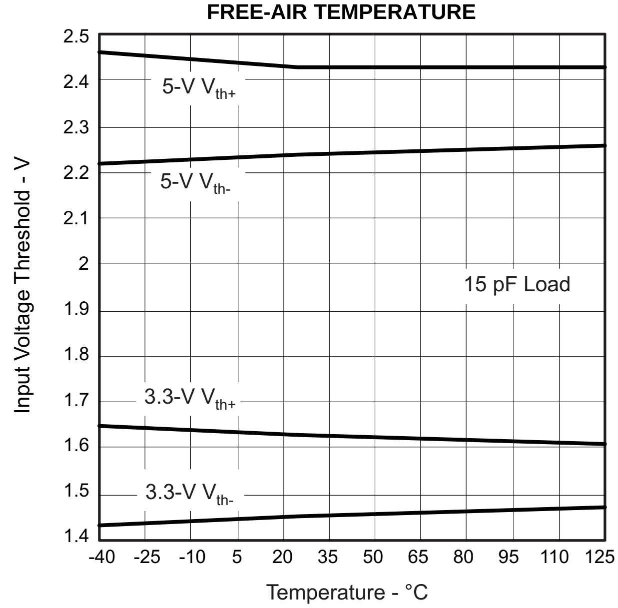


Figure 13.

TYPICAL CHARACTERISTIC CURVES (continued)

V_{CC} FAILSAFE THRESHOLD vs FREE-AIR TEMPERATURE

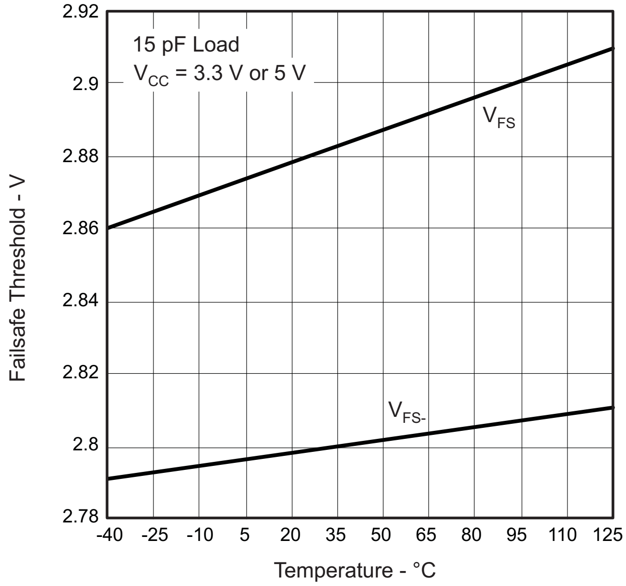


Figure 14.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

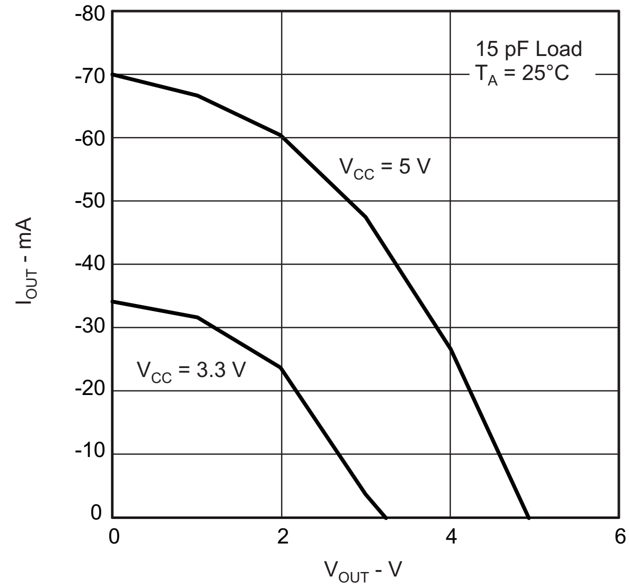


Figure 15.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

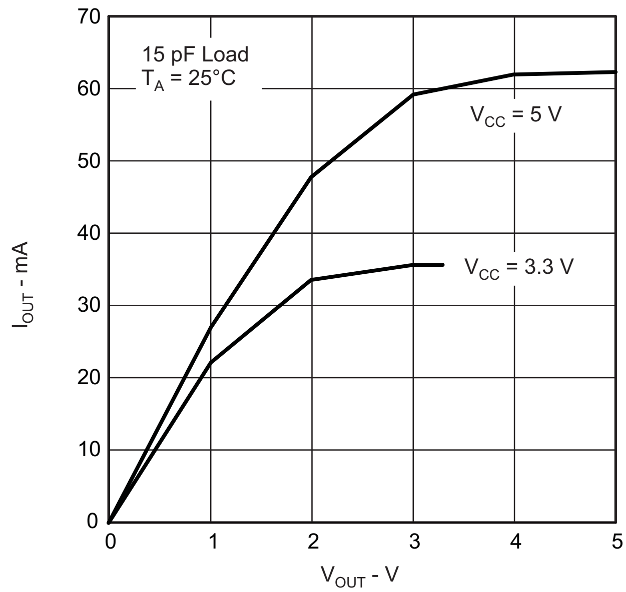


Figure 16.

ISO722xM JITTER vs SIGNALING RATE

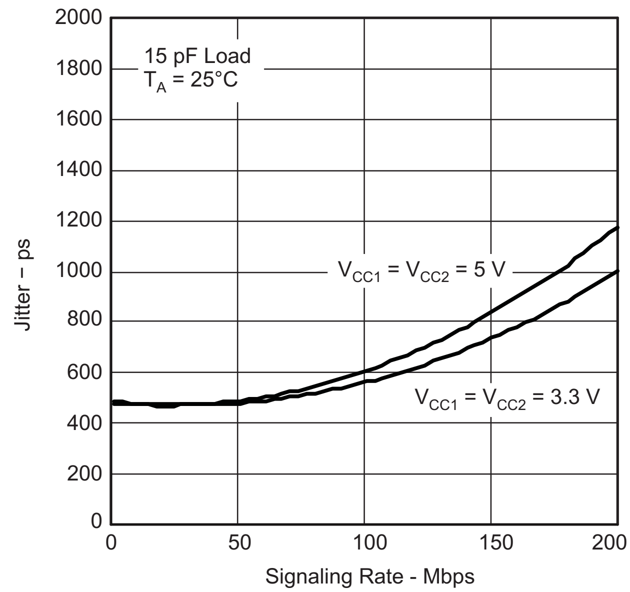


Figure 17.

APPLICATION INFORMATION

Typical Applications

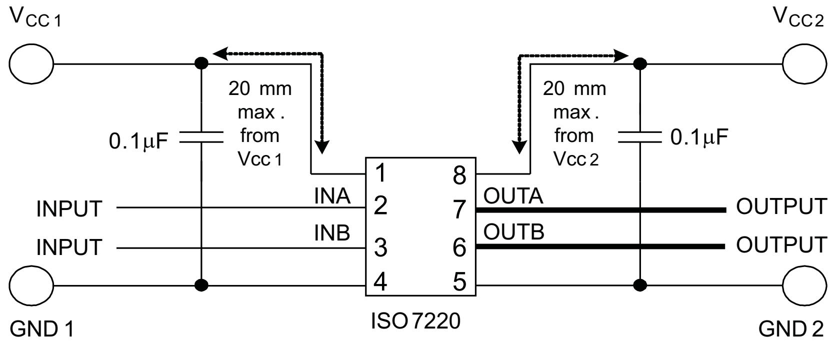


Figure 18. Typical ISO7220 Application Circuit

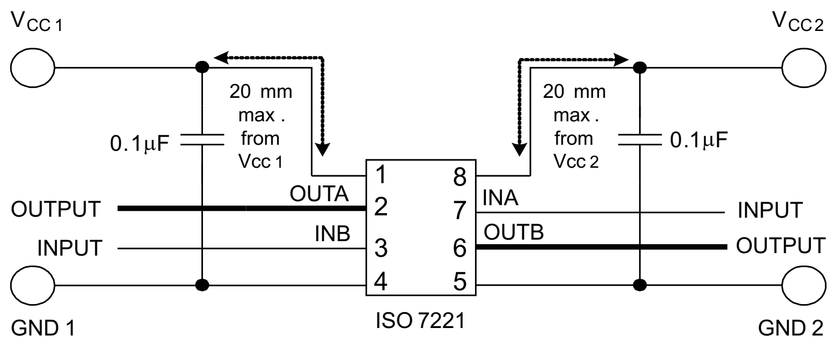


Figure 19. Typical ISO7221 Application Circuit

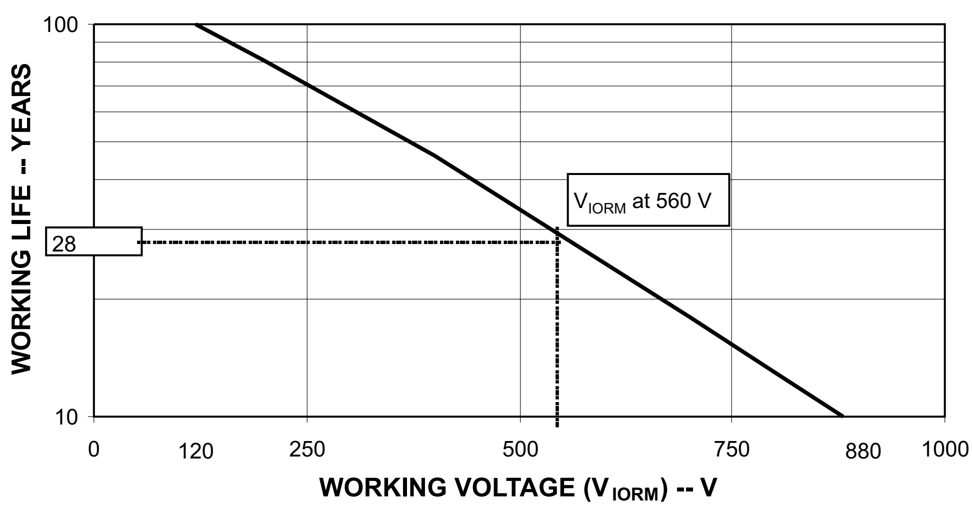
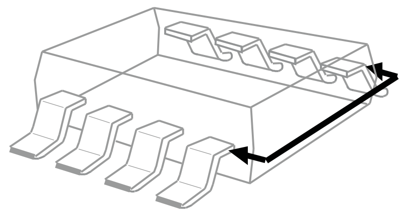


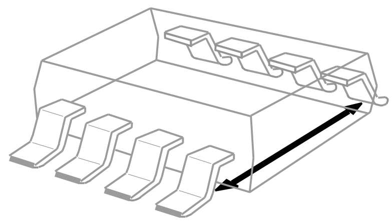
Figure 20. Time Dependent Dielectric Breakdown Test Results

ISOLATION GLOSSARY

Creepage Distance — The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance — The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to Output Barrier Capacitance — The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to Output Barrier Resistance — The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit — An internal circuit directly connected to an external supply mains or other equivalent source which supplies the primary circuit electric power.

Secondary Circuit — A circuit with no direct connection to primary power, and derives its power from a separate isolated source.

Comparative Tracking Index (CTI) — CTI is an index used for electrical insulating materials which is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

Insulation:

Operational insulation — Insulation needed for the correct operation of the equipment.

Basic insulation — Insulation to provide basic protection against electric shock.

Supplementary insulation — Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation — Insulation comprising both basic and supplementary insulation.

Reinforced insulation — A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1 — No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

Pollution Degree 2 — Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

Pollution Degree 3 — Conductive pollution occurs or dry nonconductive pollution occurs which becomes conductive due to condensation which is to be expected.

Pollution Degree 4 – Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category — This section is directed at insulation co-ordination by identifying the transient overvoltages which may occur, and by assigning 4 different levels as indicated in IEC 60664.

- I: Signal Level — Special equipment or parts of equipment.
- II: Local Level — Portable equipment etc.
- III: Distribution Level — Fixed installation
- IV: Primary Supply Level — Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ISO7220AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7220MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ISO7221CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221MDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7221MDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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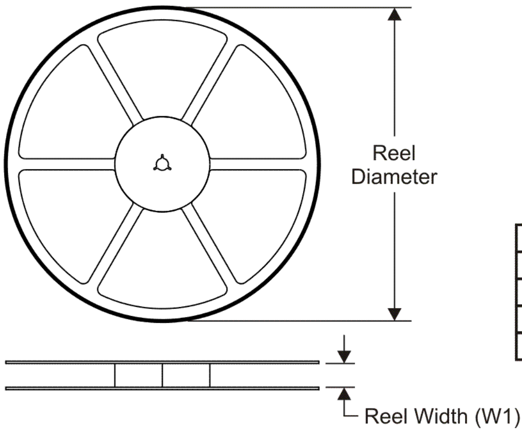
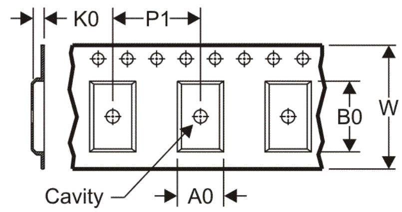
TAPE AND REEL INFORMATION

REEL DIMENSIONS

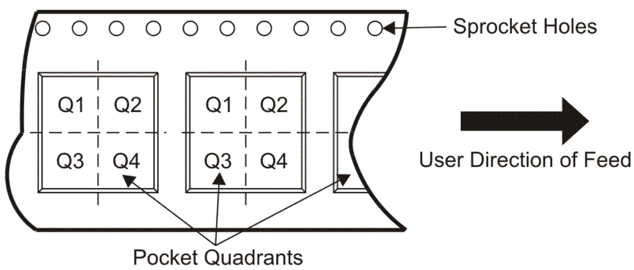


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

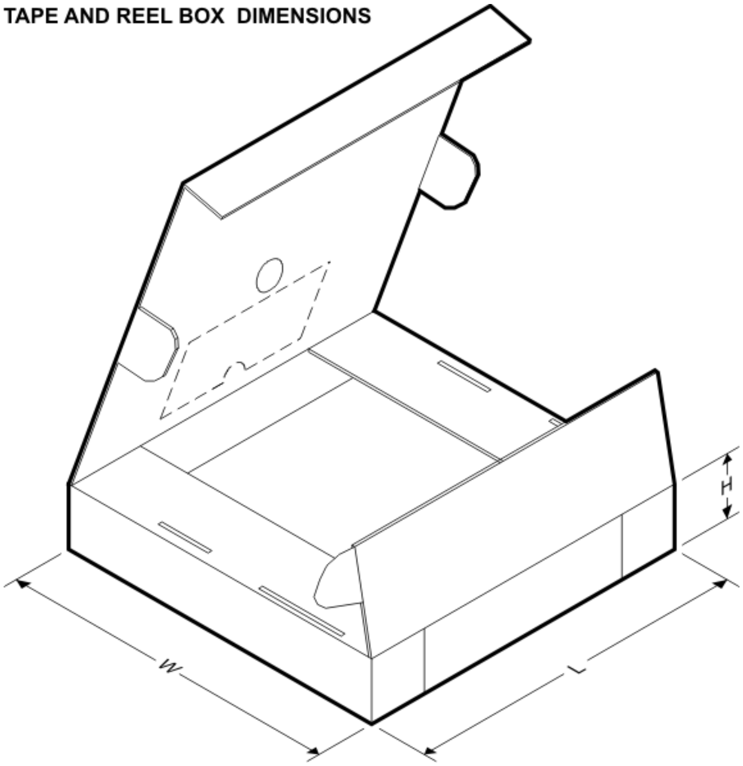
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7220ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7220MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221BDR	SOIC	D	8	2500	330.0	13.0	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7221MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

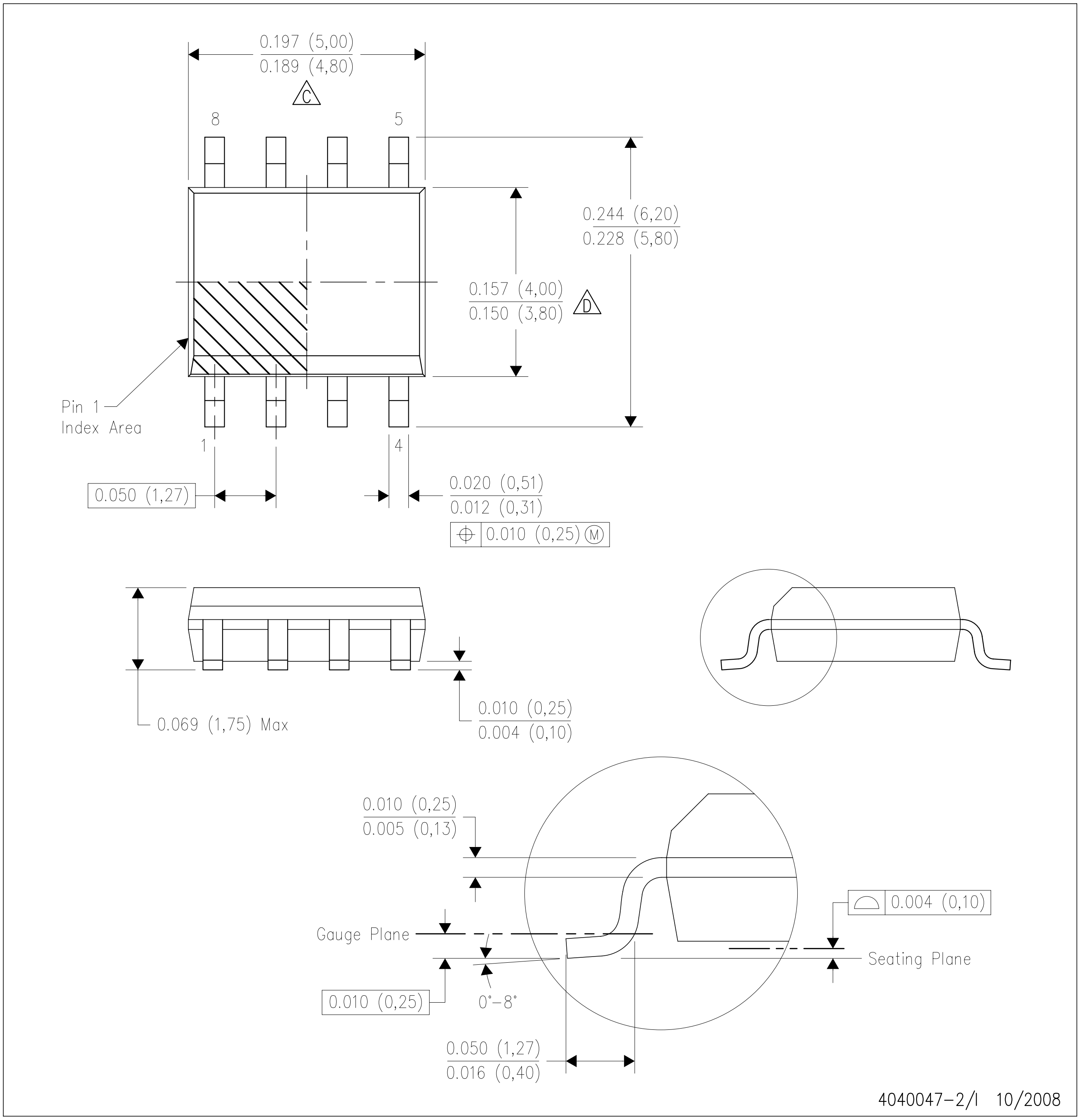
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7220ADR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7220BDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7220CDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7220MDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7221ADR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7221BDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7221CDR	SOIC	D	8	2500	358.0	335.0	35.0
ISO7221MDR	SOIC	D	8	2500	358.0	335.0	35.0

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

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